IN THE CLAIMS:

Claims 1-5 and 8-16 were previously cancelled. Claims 17 through 22 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1.-5. (Cancelled)

16. (Previously presented) A method of forming a gate stack, comprising:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting the polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop the polysilicon layer; and
depositing a dielectric cap layer over the metallic silicide film at a temperature below about 600°C, wherein the temperature is sufficiently low to maintain the metallic silicide film in the non-annealed state.

17. (Previously presented) A method of forming a gate stack, comprising:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting the polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop the polysilicon layer; and
depositing a dielectric cap layer over the metallic silicide film at a temperature below about 600°C, wherein the temperature is sufficiently low to preclude formation of silicon clusters in the metallic silicide film.

8.-16. (Cancelled)

3 17. (Currently amended) A method for forming a gate stack, comprising:
providing a semiconductor substrate with a dielectric layer on an active surface of ~~said~~ the semiconductor substrate, wherein a polysilicon layer is disposed over ~~said~~ the dielectric layer;
forming a metallic silicide film in a non-annealed state over ~~said~~ the polysilicon layer;
forming a dielectric cap on ~~said~~ the metallic silicide film at a sufficiently low temperature so that ~~said~~ the metallic silicide film remains in ~~said~~ the non-annealed state;
forming and patterning a resist layer on ~~said~~ the dielectric cap;
etching ~~said~~ the dielectric cap, ~~said~~ the metallic silicide film, and ~~said~~ the polysilicon layer; and
stripping ~~said~~ the resist layer.

4 ~~18.~~ (Currently amended) The method of claim 3 ~~17~~, wherein forming ~~said~~ the dielectric cap is effected at a temperature below about ~~600° C.~~ 600°C.

5 ~~19.~~ (Currently amended) A method of forming a gate stack, consisting essentially of:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting ~~said~~ the polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop ~~said~~ the polysilicon layer; and
depositing a dielectric cap layer over ~~said~~ the metallic silicide film at a temperature below about 600°C such that the metallic silicide film remains in ~~said~~ the non-annealed state.

6 ~~20.~~ (Currently amended) The method of claim ~~19~~, wherein ~~said~~ the depositing a dielectric cap layer over ~~said~~ the metallic silicide film is effected at a temperature of between 400°C and 600°C.

7 21. (Currently amended) The method of claim 5 19, wherein ~~said~~ the depositing a dielectric cap layer over ~~said~~ the metallic silicide film is effected at a temperature of about 500°C.

E1 8 22 (Currently amended) The method of claim 5 19, wherein ~~said~~ the depositing a dielectric cap layer over ~~said~~ the metallic silicide film is effected at a temperature sufficiently low to preclude formation of silicon clusters in ~~said~~ the metallic silicide film.